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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Application Number	10/656,982
Filing Date	9/5/2003
First Named Inventor:	Shashi B. Sakhuja
Examiner: Unknown ENGELAND	GROUP: 2818 2816

Sheet	1	of	1	Attorney Docket Number	CAT-00001
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U.S. PATENT DOCUMENTS

Examiner Initials*	Cited No. ¹	Document Number Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
TLE	A01	US-5,309,009	05/1994	Chao	257/318
TLE	A02	US-5,963,084	10/1999	Eschauzier	327/553
TLE	A03	US-6,133,780	10/2000	Chi	327/541
TLE	A04	US-6,297,689	10/2001	Merrill	327/540
TLE	A05	US-6,414,536	07/2002	Chao	327/540

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Cntry Code ³ Number ⁴ Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear	T ⁶

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)EXAMINER SIGNATURE: Tommy L. EnglandDATE CONSIDERED: 1/3/05

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Application Number		Filed Herewith 10/656,982			
		Filing Date		September 5, 2003			
		First Named Inventor:		Shashi B. Sakhuja			
		Examiner name: unknown ENGLAND		GROUP: unknown 2816			
Sheet	1	of	1	Attorney Docket Number CAT-00001			
U.S. PUBLISHED PATENT APPLICATIONS							
Examiner Initials*	Cited No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Info. Appear	
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TLE	A01	5495453		Wociechowski et al.	02/27/1996		
TLE	A02	5901085		Kramer et al.	05/04/1999		
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		Office ³ Number ⁴	Kind Code ⁵ (if known)				
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
TLE	Harrison et al.: "A CMOS :Programmable Analog Memory-Cell Array Using Floating Gate Circuits"; IEEE 2001; IEEE Transactions On Circuits And Systems-II: Analog And Digital Signal Processing, Vol. 48, No. 1, January 2001. pp. 4-11.						
EXAMINER <i>Tony England</i>		DATE CONSIDERED 1.13.05					

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